EiE Firmware I Development Board: EIEFI-01

Block Diagram and PCB Labels

Title: Block Diagram and PCB Labels
Number: EIEFI-SCH
Version: 01
Author: JRL
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PCB Revision

U_Sheet1
EIEF1-SCH Sheet1.SchDoc

U_Sheet2
EIEF1-SCH Sheet2.SchDoc

U_Sheet3
EIEF1-SCH Sheet3.SchDoc

U_Sheet4
EIEF1-SCH Sheet4.SchDoc

U_Sheet5
EIEF1-SCH Sheet5.SchDoc

U_MPGL1-EHDW-03 Release Notes
EIEF1-01 Release Notes.SchDoc
5V USB Input

Note: 5V rail will be ~4.7V due to D9 and may not meet spec of some Blade daughter boards; for full 5V power from J2

VCC Regulator: 3.3V Output

3.27V 300mA
C6 10uF 0805

D9
1N5819HW-7-F

R1 10k

R3 69k

R4 100k

C4 1uF

C5 1uF

C6 10uF 0805

D1 MMSD4148T3G

D2 MMSD4148T3G

BAT1 CR2032 NNP

5V_USB1

USB_JLINK_P

USB_JLINK_N

TP1 5V

GND

5V

USB_DATA_N

USB_DATA_P

J2 MICRO AB

DATA / POWER

USB_JLINK_P

USB_JLINK_N

TP1 5V

GND

5V

USB_DATA_N

USB_DATA_P

J1 MICRO AB

J-LINK OB

D19

Note: 5V rail will be ~4.7V due to D9 and may not meet spec of some Blade daughter boards; for full 5V power from J2
-02 to -03 updates (MPG):
  Lower cost dual RS232 driver
  RGB LEDs for expensive colors / configurable
  Remove fuse & power switch and diode connect J-Link power (for true 5V, use PWR/DATA in port)
  Switch for SWCLK and SWDIO for ANT programming.
  Change micro B USB to pinned versions
  Bumpon circles x 4

EIEF1-01 Updates
  Swap DEBUG_PIMO and DEBUG_POMI into J-Link OB
  Add J4 for direct nRF51422 programming / debugging
  Connect two existing nRF51422 test points in to new J4 for optional UART access
  Add S3 (RESET) footprint TL3301 for future cost reduction
  Add X5 low cost 32k crystal for future cost reduction
  Update J7 schematic symbol
  BOM: Remove J5 (DB9), C46-C50, and U7 (RS-232)
  BOM: R21 390R to 150R for brighter blue
  BOM: R60 and R61 now populated for debug UART to J-Link OB
  BOM: R1 and R58 to 10k to dim status LEDs
  BOM: R62 to NNP (enables J-Link CDC)

Considered but not implemented:
  LCD flat on board