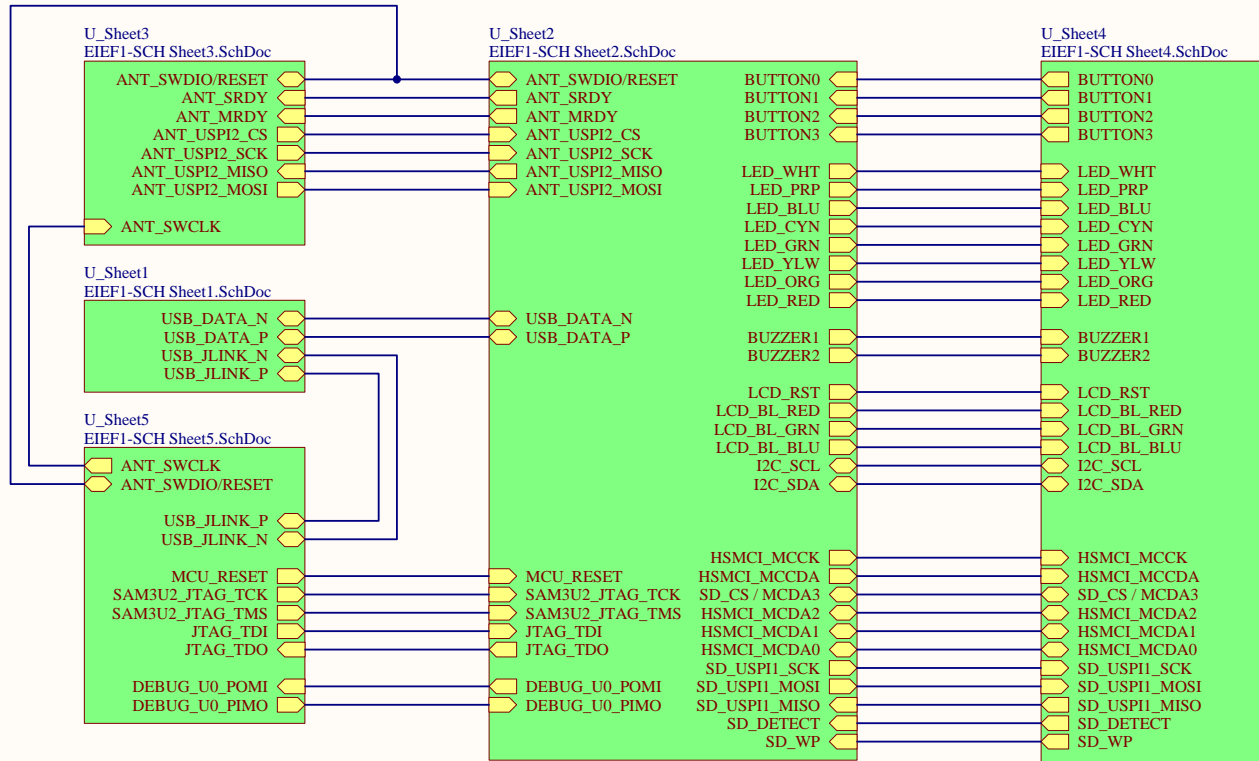


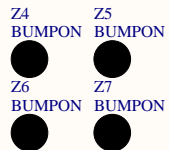
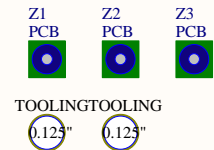
# EiE Firmware I Development Board: EIEFI-OI



U\_MPGL1-EHDW-03 Release Notes  
EIEFI-01 Release Notes.SchDoc

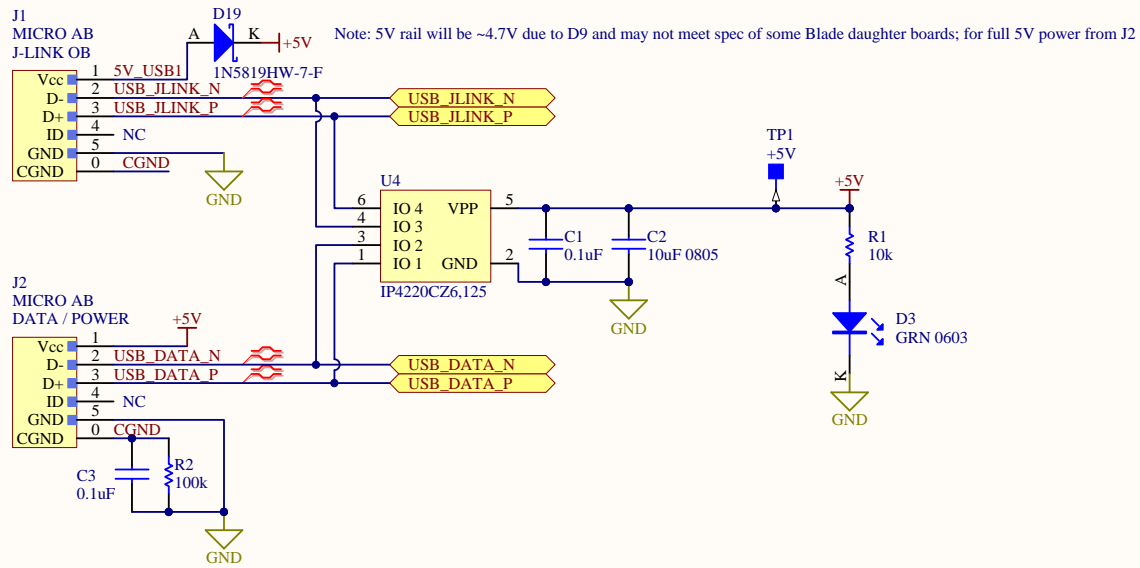


LBL6  
PCB Revision  
PCB REV

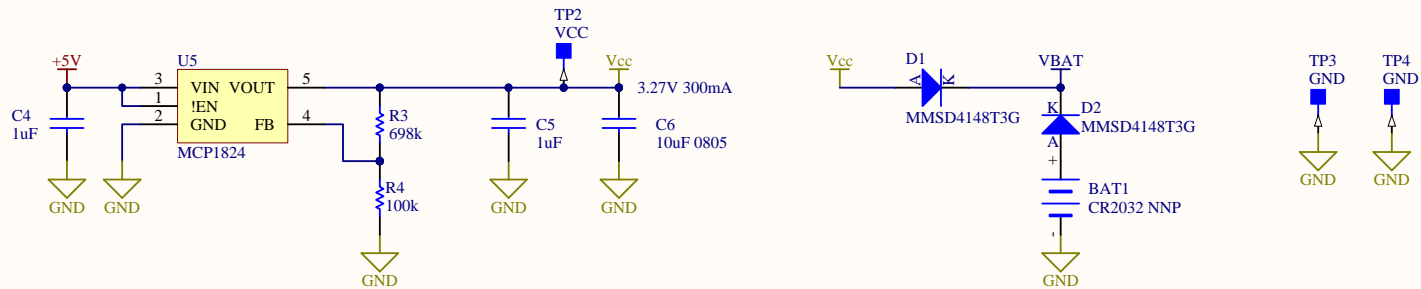


 5831 DALFORD RD NW CALGARY AB T3A 1L3 CANADA 1-888-912-3451	Title: <b>Block Diagram and PCB Labels</b>		
	Number: EIEFI-SCH	Version: 01	Author: JRL
	Date: 8/11/2016	Sheet: 0 of 5	
	File: EIEFI-SCH Main.SchDoc		

## 5V USB Input



## VCC Regulator: 3.3V Output



A

A

B

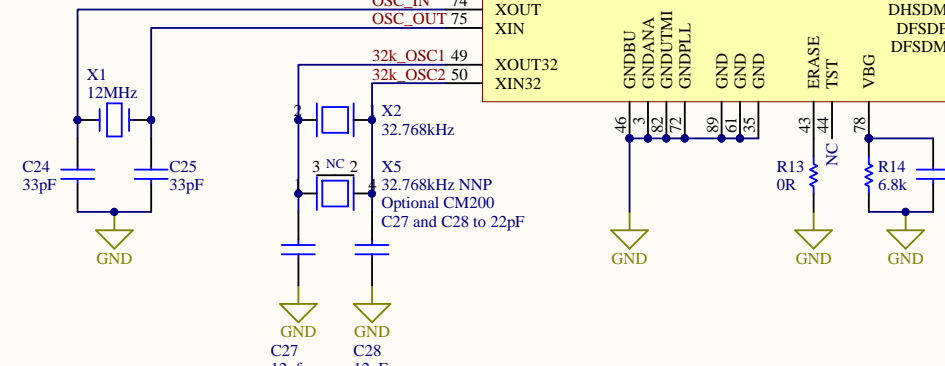
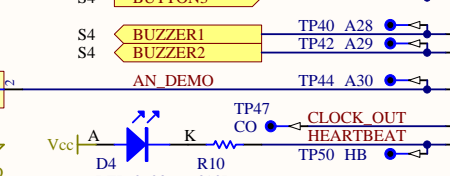
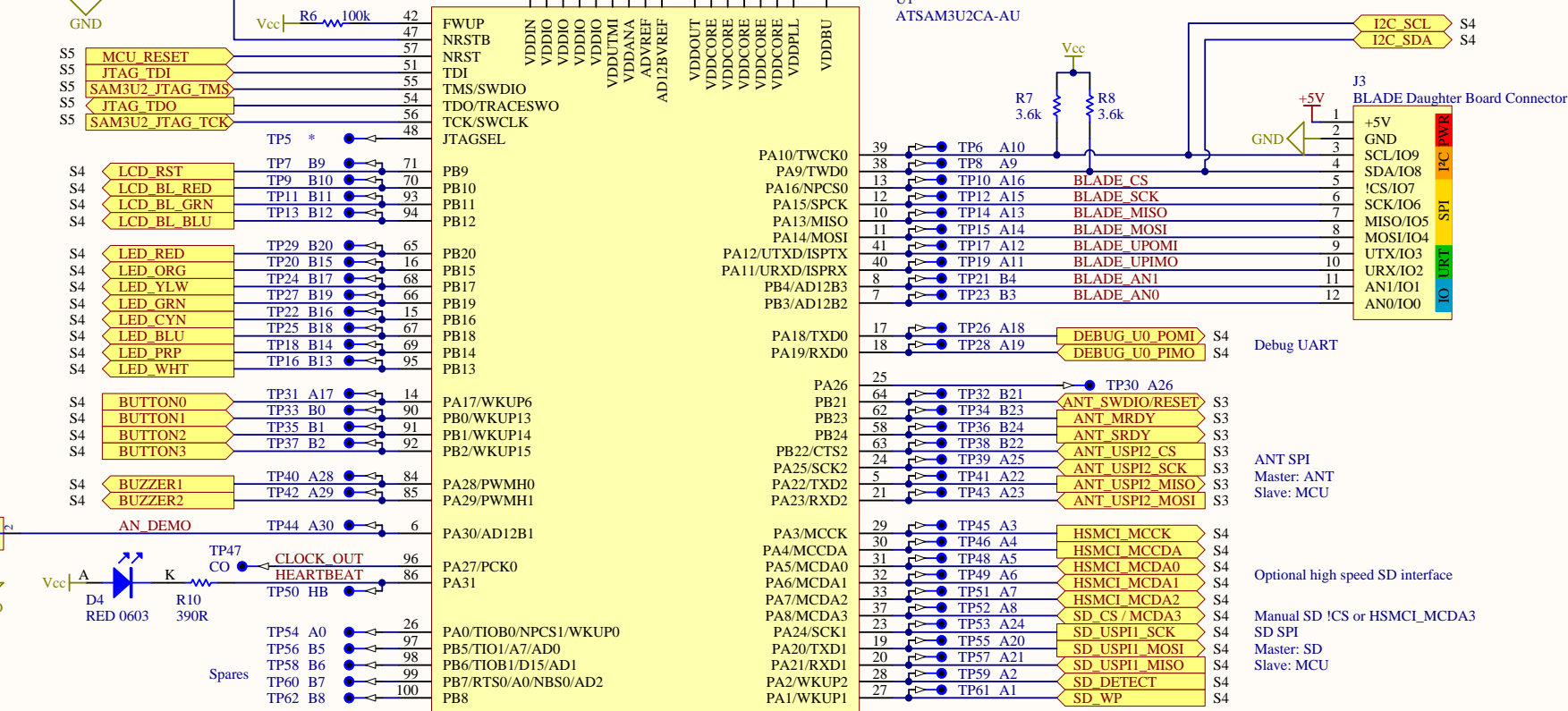
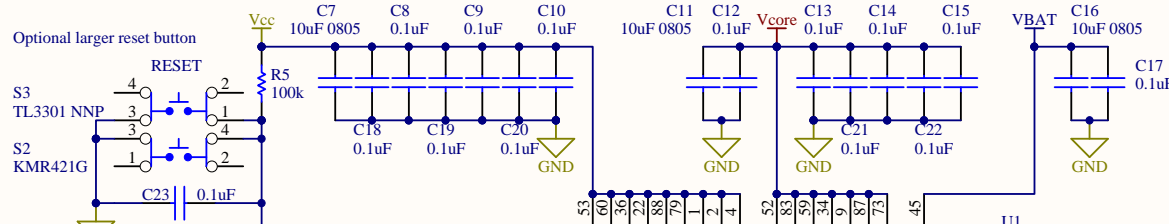
B

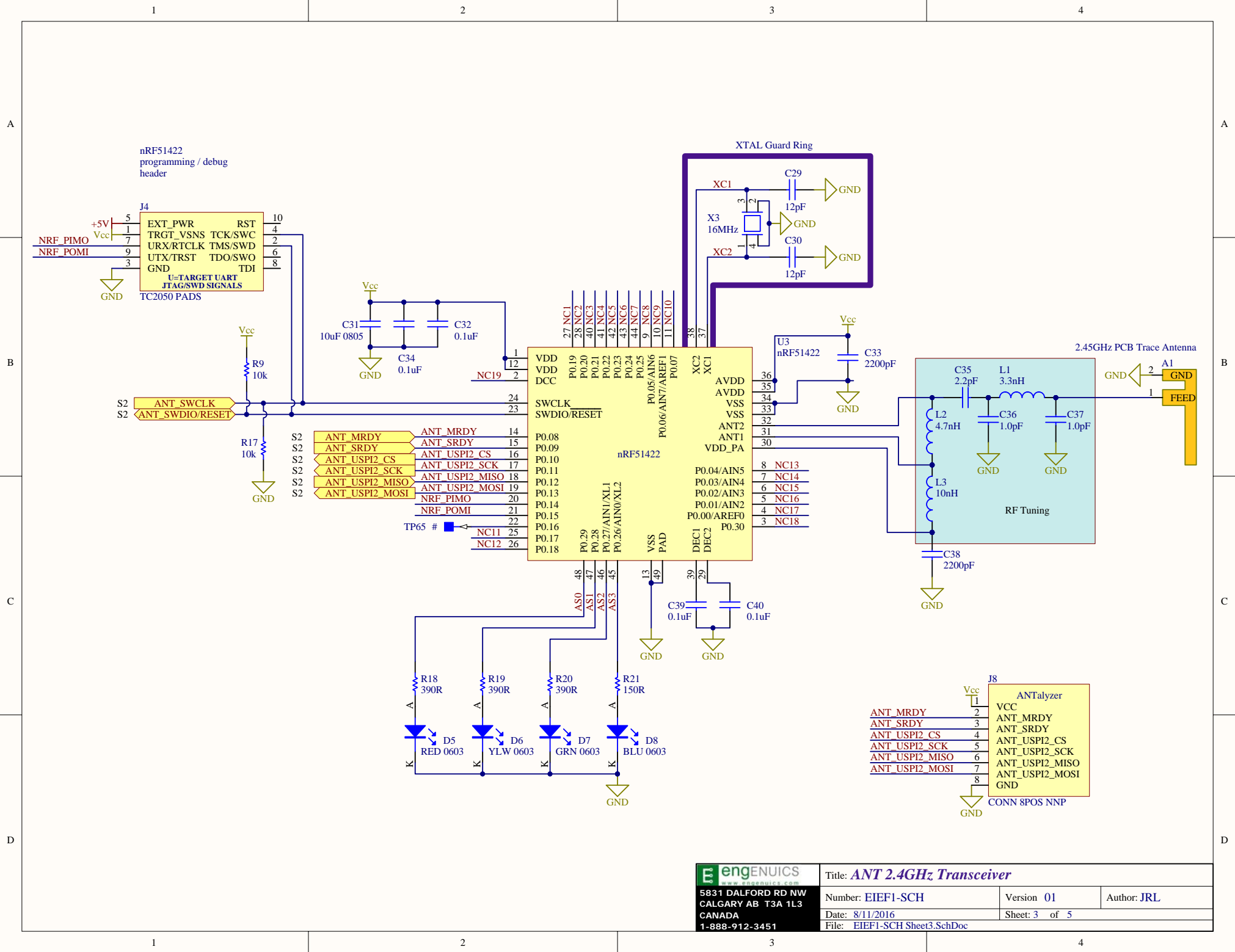
C

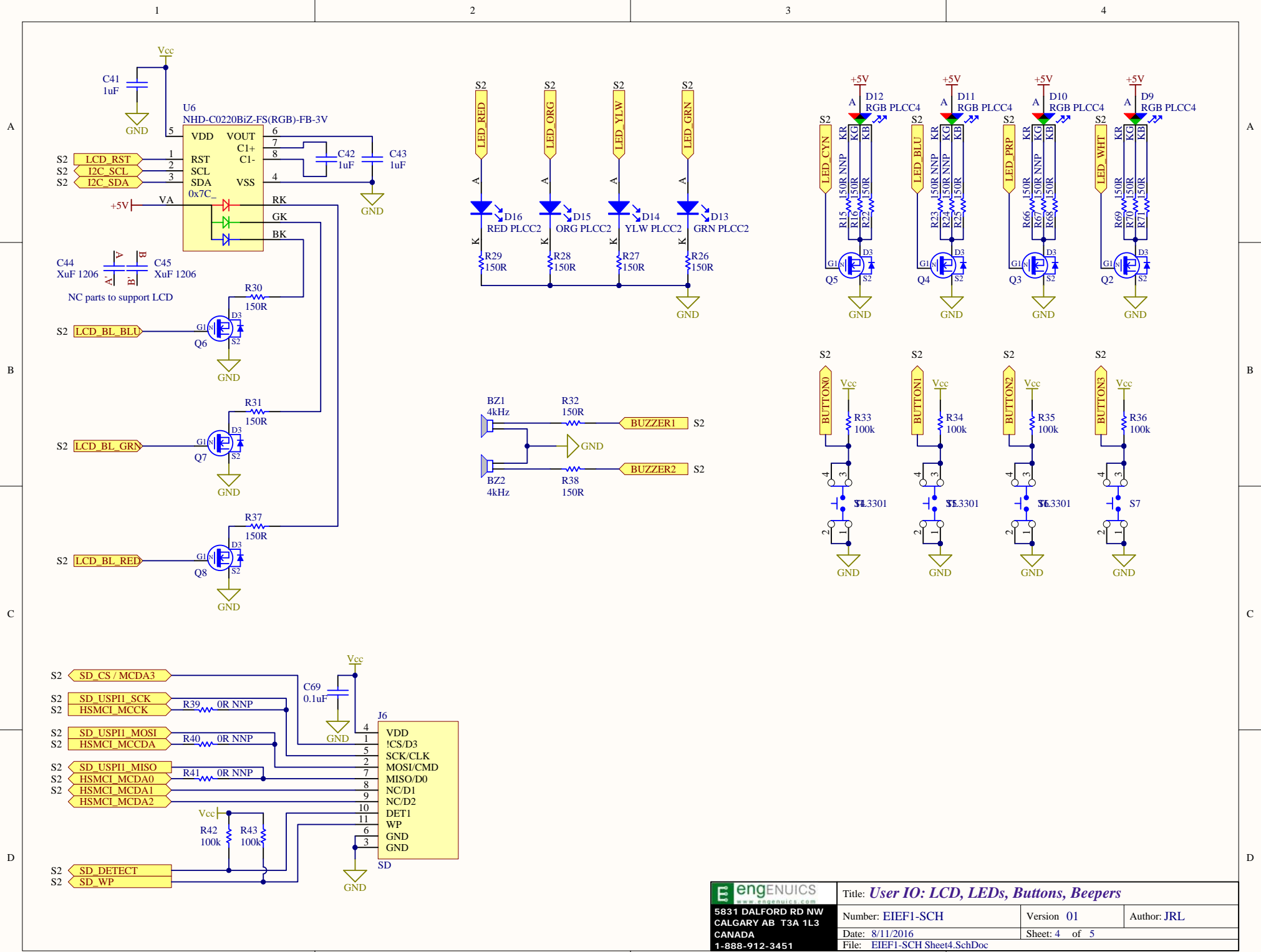
C


D

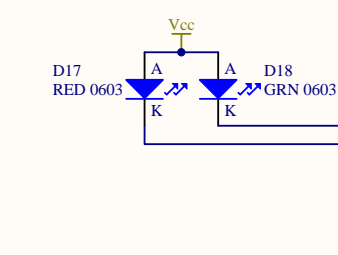
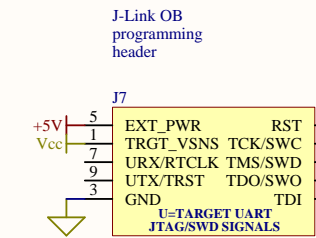
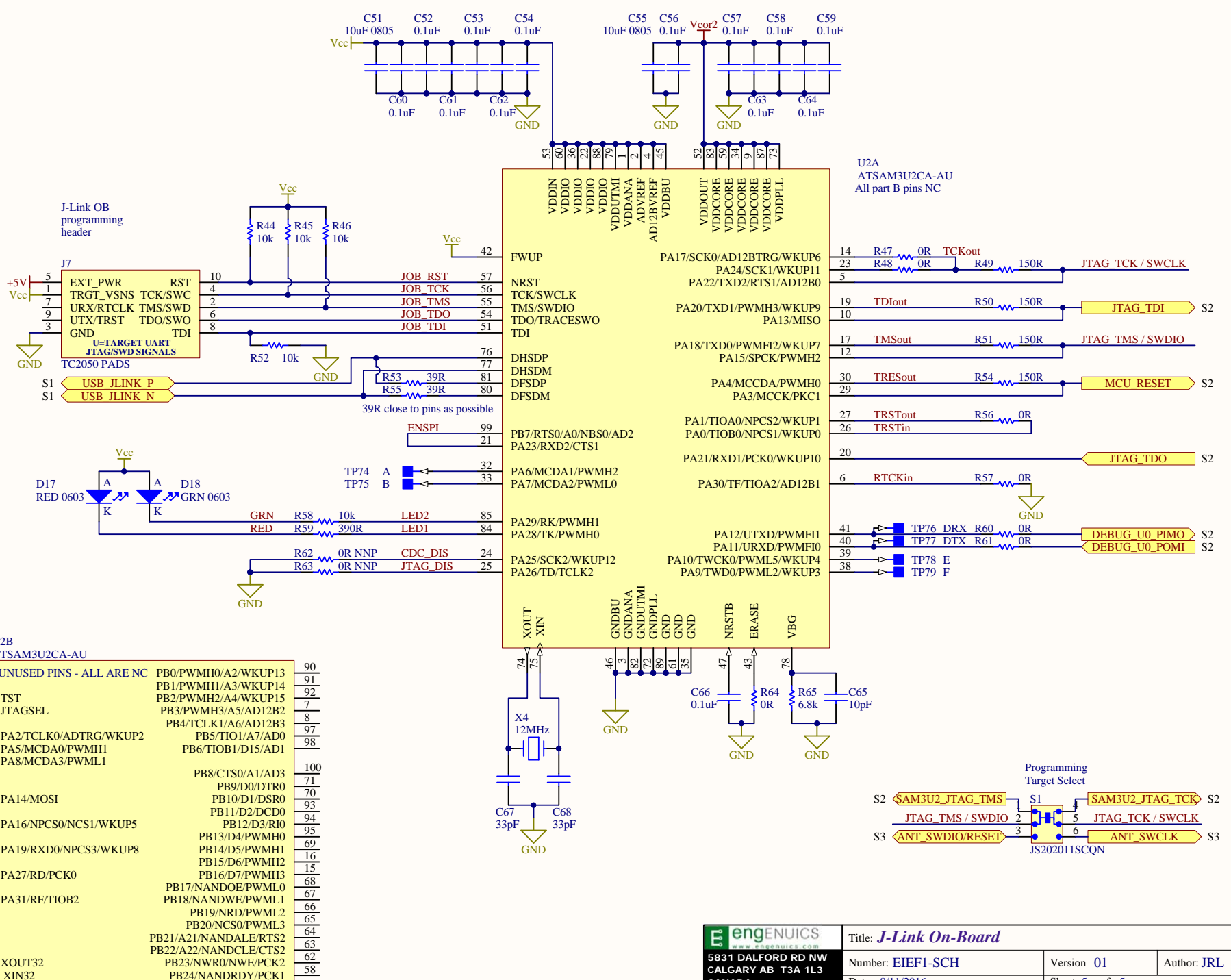
D







 5831 DALFORD RD NW CALGARY AB T3A 1L3 CANADA 1-888-912-3451	Title: <b>User IO: LCD, LEDs, Buttons, Beepers</b>		
	Number: EIEF1-SCH	Version 01	Author: JRL
	Date: 8/11/2016	Sheet: 4 of 5	
	File: EIEF1-SCH Sheet4.SchDoc		



U2B  
ATSAM3U2CA-AU

44	UNUSED PINS - ALL ARE NC	90
48	TST	91
	JTAGSEL	92
28	PA2/TCLK0/ADTRG/WKUP2	7
31	PA5/MCDA0/PWMH1	8
37	PA8/MCDA3/PWML1	8
	PB8/CTS0/A1/AD3	100
11	PA14/MOSI	71
	PB9/D0/DTR0	70
13	PA16/NPCS0/NCS1/WKUP5	93
	PB10/D1/DSR0	94
18	PA19/RXD0/NPCS3/WKUP8	95
	PB11/D2/DCD0	96
96	PA27/RD/PCK0	97
	PB12/D3/R10	98
86	PA31/RF/TIOB2	99
	PB13/D4/PWMH0	97
	PB14/D5/PWMH1	98
	PB15/D6/PWMH2	99
	PB16/D7/PWMH3	100
	PB17/NANDOE/PWML0	71
	PB18/NANDWE/PWML1	70
	PB19/NRD/PWML2	93
	PB20/NCS0/PWML3	94
	PB21/A21/NANDALE/RTS2	95
	PB22/A22/NANDCLE/CTS2	96
49	XOUT32	69
50	XIN32	16
	PB23/NWR0/NWE/PCK2	15
	PB24/NANDRDY/PCK1	68
		67
		66
		65
		64
		63
		62
		61
		60
		59
		58

-02 to -03 updates (MPG):

- Lower cost dual RS232 driver
- RGB LEDs for expensive colors / configurable
- Remove fuse & power switch and diode connect J-Link power (for true 5V, use PWR/DATA in port)
- Switch for SWCLK and SWDIO for ANT programming.
- Change micro B USB to pinned versions
- Bumpon circles x 4

Considered but not implemented:  
LCD flat on board

A

A

EIEF1-01 Updates

- Swap DEBUG\_PIMO and DEBUG\_POMI into J-Link OB
- Add J4 for direct nRF51422 programming / debugging
- Connect two existing nRF51422 test points in to new J4 for optional UART access
- Add S3 (RESET) footprint TL3301 for future cost reduction
- Add X5 low cost 32k crystal for future cost reduction
- Update J7 schematic symbol
- BOM: Remove J5 (DB9), C46-C50, and U7 (RS-232)
- BOM: R21 390R to 150R for brighter blue
- BOM: R60 and R61 now populated for debug UART to J-Link OB
- BOM: R1 and R58 to 10k to dim status LEDs
- BOM: R62 to NNP (enables J-Link CDC)

B


B

C

C

D

D

 5831 DALFORD RD NW CALGARY AB T3A 1L3 CANADA 1-888-912-3451	Title: <i>Release Notes</i>		
	Number: EIEF1-SCH	Version: 01	Author: JRL
	Date: 8/11/2016	Sheet: R of R	
	File: EIEF1-01 Release Notes.SchDoc		